SO-CFP-ER4

CFP, 103/112 Gbps, SM, DDM, 40 km

OVERVIEW

The SO-CFP-ER4 is a 100G transceiver module supporting 100GBASE-ER4 and ITU-T OTU-4 applications over single mode (SM) fiber. It has a transmission distance of 40km The module is designed with form factor, optical/electrical connection and digital diagnostic interface according to the CFP MSA Hardware Specification Revision 1.4.

PRODUCT FEATURES

- 4-lane x 25.78Gb/s L-WDM optical interface
    - High quality and reliability optical sub-assemblies
    - 1300nm cooled WDM EA-DFB transmitter with optical MUX
    - High sensitivity PIN-TIA with optical DEMUX
    - Low noise and low distortion SOA
    - 1300nm band with 800GHz spacing LAN WDM grid up to 40km over a SMF
- IEEE802.3ba compliant
    - IEEE802.3 Clause 88 100GBASE-ER4
    - CAUI(10x10G) electrical interface
    - MDIO interface for module management
    - OTU-4 rate operation
    - 4x27.95 Gb/s lane operation to support OTU-4
    - ITU-T 4L1-9C1F compatible 40km optical I/F option available
- Compliant with CFP MSA specification
    - Easy supply management for hot-pluggability
    - CFP MSA form factor
    - 148pin electrical connector
    - Duplex SC or LC receptacle
- Low power consumption
    - 3.3V single power supply, 18W max
- RoHS compliant applications

ORDERING INFORMATION

Part Number	Description
SO-CFP-ER4	CFP, 103/112 Gbps,1300nm, SM, DDM, 40km, angled LC
SO-CFP-ER4-LC	CFP, 103/112 Gbps,1300nm, SM, DDM, 40km, flat LC
SO-CFP-ER4-SC	CFP, 103/112 Gbps,1300nm, SM, DDM, 40km, flat SC

FUNCTIONAL DIAGRAM

The SO-CFP-ER4 CFP transceiver is a bi-directional module with a transmitter and receiver in one package. The SO-CFP-ER4 contains a duplex SC or LC connector for the optical interface and a 148-pin connector for the electrical interface. SO-CFP-ER4 contains electrical 10:4 Mux, 4:10 de-MUX, 4-lane optical transmitter, 4-lane optical receiver and module management block including MDIO interface. The transceiver module receives 10-lane 10.3Gb/s CAUI electrical inputs. CDR reshapes and retimes received electrical signal to compensate the degraded electrical signal which comes through host board and host connectors. A reference clock from host card is 1/64 frequency of TX CAUI lane rate and should be synchronized to TX CAUI input signal. 10 to 4 electrical Mux synthesizes 4-lane rate clock from the reference clock and multiplexes 10-lane received signals to 4-lane electrical signals. The multiplexed 4-lane signals are fed to the transmitters. The four transmitters convert 4-lane signals to an optical signal through 4 Laser drivers and Lasers diodes. Each Laser launches optical signal in specific wavelength specified in IEEE802.3ba 100GBASE-ER4 requirements. These 4-lane optical signals will be optically multiplexed into one fiber by 4 to1 Optical WDM MUX. The optical output power is held constant by an automatic power control (APC) circuit. The transmitters output can be turned off by TX_DIS hardware signal and/or through MDIO module management Interface. The SO-CFP-ER4 receives 4-lane LAN WDM optical signals. The optical signals are amplified to the proper received signal level by SOA. This amplified signals are de-multiplexed by 1 to 4 optical DEMUX and fed into each Receiver Optical Sub-Assembly that converts optical to electrical signal. The regenerated electrical signals are retimed and de-jittered by the CDRs inside the 4:10 electrical DeMuX. The retimed 4-lane received signals are de-multiplex to 10-lane signals by the 4 to 10 electrical DeMux. The 10-lane signals are compliant with IEEE CAUI interface requirements. Each received optical signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be launched. The SO-CFP-ER4 supports the MDIO interface specified in IEEE802.3 Clause 45. This 2-wire management data I/O interface is provided for the module status monitoring and control. The management data clock (MDC) provides clocking for the data that is passed on the MDIO port. Five further pins allow for loading of a port address (PORT_ADDR0-4) into the module.

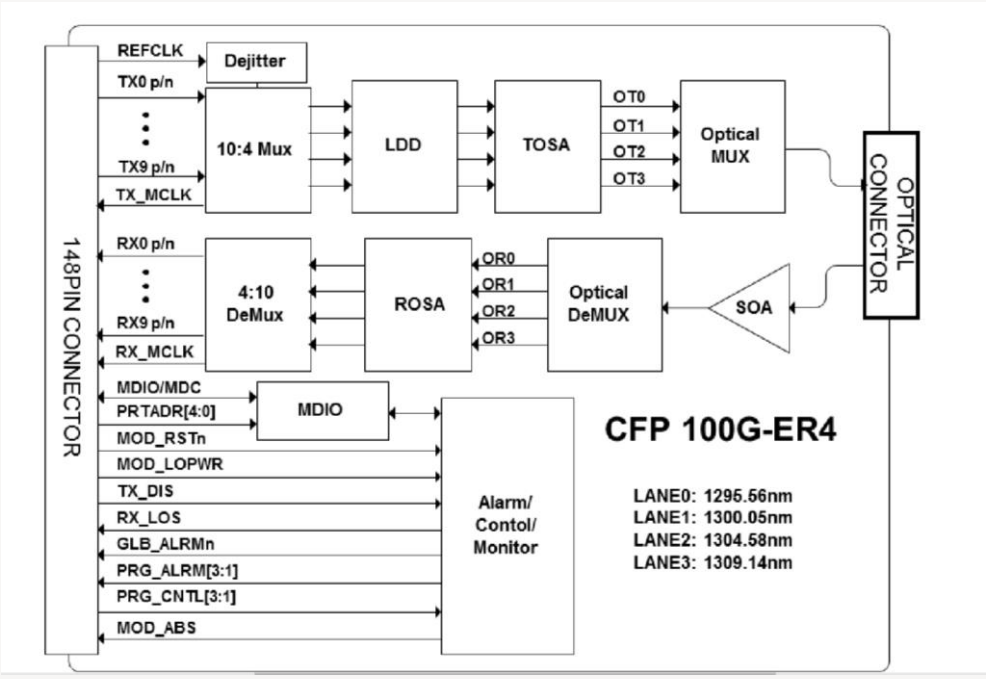


Figure 1. Functional diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit

Storage Temperature	*Ts*	-40	+85	°C
Supply Voltage	Vcc	-0.3	3.6	V
Operating Relative Hunidity	*RH*		85	%

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T_c	-5		70	°C
Power Supply Voltage	*Vcc*	3.135	3.3	3.465	V
Power Consumption	P			18	W
Baud rate			103	112	Gbps
Link Distance (SM fiber)				40	km

ELECTRICAL CHARACTERISTICS – TRANSMITTER & RECEIVER (EACH LANE)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Transmitter						
Input Amplitude (Differential)	V_{in}	400		1200	mVpp	AC coupled inputs
Differential Input Impedance	Z_{in}	80	100	120	Ohm	Rin > 100kOhm @ DC
Receiver						
Output Amplitude (Differential)	V_{out}	360		770	mVpp	AC coupled outputs
Differential Output Impedance	Z_{out}	80	100	120	Ohm	

MDIO INTERFACE SPECIFICATION

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input Voltage	V_{IH}	0.84		1.5	V	
	V_{IL}	-0.3		0.36	V	
Input Leak current	I_{IN}	-100		100	µA	
Output Voltage	V_{OH}	1.0		1.5	V	
	V_{OL}	-0.3		0.2	V	
Input Capacitance	C_I			10	pF	
Input MDC Clock	f_{MDC}	0.1		4	MHz	
MDC Clock Period	T_{MDC}	250		10000	nsec	
MDIO Hold Time	T_{hold}	10			nsec	
MDIO Setup Time	T_{setup}	10			nsec	
GLB_ALM	$T_{glb\_alm\_ass}$					
	$T_{glb\_alm\_dea}$					

OPTICAL CHARACTERISTICS – TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Host Native Nominal Bit Rate			10x 10.3125 (CAUI) & 4x 27.9525 (OTU4)		Gbps	

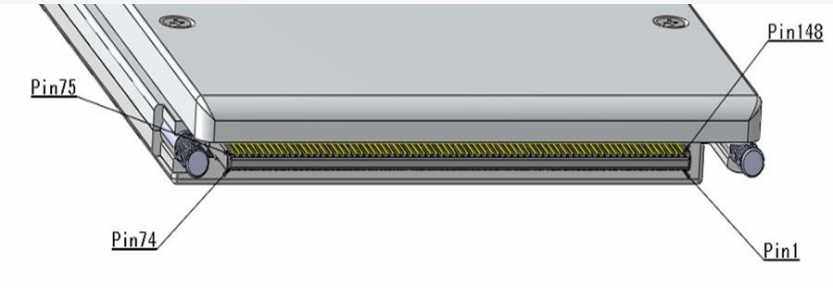
DWDM Line Interface Bit Rate			4x 25.78125 (4 Lane 100GE) & 4x 27.9525 (OTU4)		Gbps
OTN Interface Bit Rate Deviation			±20		ppm
CAUI Interface Bit Rate Deviation			±100		ppm
Lane wavelength (range): L0	L0	1294.53	1295.56	1294.53	nm
Lane wavelength (range): L1	L1	1299.02	1300.05	1301.09	nm
Lane wavelength (range): L2	L2	1303.54	1304.58	1305.63	nm
Lane wavelength (range): L3	L3	1308.09	1309.14	1310.19	nm
Single mode suppression ratio	SM SR	30			dB
Total average launch power (max)	P_{ot}		8.9		dBm
Average launch power, each lane (max)	P_{avemax}		2.9		dBm
OMA, each lane (max)	OMA	0.1		4.5	dBm
Difference power (OMA and averaged) between any two lanes	ΔP			3.6	dBm
Transmitter and Dispersion Penalty (TDP), each lane	TDP			2.5	dB
Average power Disabled, each lane	P_{OFF}			-30	dBm
Extinction Ratio	ER	8	9		dB
Optical Return Loss Tolerance	RLT			20	dB

OPTICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Damage threshold	P_D		-	5.5	dBm	
Average receive power, each lane	P_{in}			4.5	dBm	
Receive power, each lane (OMA)	P_{OMAMAX}			4.5	dBm	
Receiver reflectance	R			-26	dBm	
Receiver sensitivity (OMA), each lane	RS			-21.4	dBm	
Rx-Lane LOS Assert	LOS_a		-33		dBm	
Rx-Lane LOS Deassert	LOS_d		-31		dBm	
Rx-Lane LOS Hysteresis	LOS_h	0.5			dB	

PIN ASSIGNMENT AND FUNCTION DEFINITIONS

PIN ASSIGNMENT



PIN DEFINITION

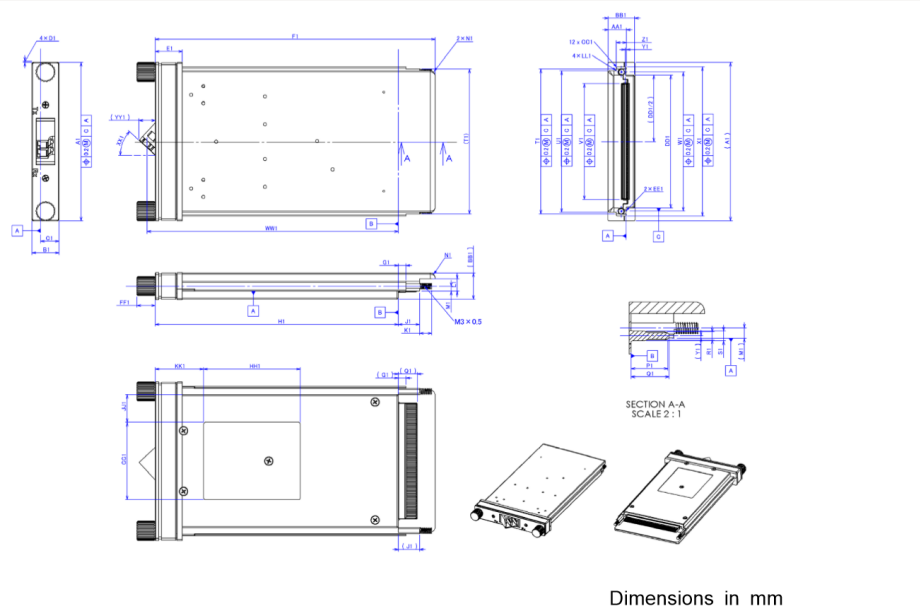
PIN	Signal Name	Description	PIN	Signal Name	Description
1	GND	3.3V Module Supply Ground	148	GND	3.3V Module Supply Ground
2	GND	3.3V Module Supply Ground	147	REFCLKn	Reference Clock Input
3	GND	3.3V Module Supply Ground	146	REFCLKp	Reference Clock Input
4	GND	3.3V Module Supply Ground	145	GND	3.3V Module Supply Ground
5	GND	3.3V Module Supply Ground	144	NC	Not Connected
6	3.3V	3.3V Module Supply Voltage	143	NC	Not Connected
7	3.3V	3.3V Module Supply Voltage	142	GND	3.3V Module Supply Ground
8	3.3V	3.3V Module Supply Voltage	141	TX9n	CML Input
9	3.3V	3.3V Module Supply Voltage	140	TX9p	CML Input
10	3.3V	3.3V Module Supply Voltage	139	GND	3.3V Module Supply Ground
11	3.3V	3.3V Module Supply Voltage	138	TX8n	CML Input
12	3.3V	3.3V Module Supply Voltage	137	TX8p	CML Input
13	3.3V	3.3V Module Supply Voltage	136	GND	3.3V Module Supply Ground
14	3.3V	3.3V Module Supply Voltage	135	TX7n	CML Input
15	3.3V	3.3V Module Supply Voltage	134	TX7p	CML Input
16	GND	3.3V Module Supply Ground	133	GND	3.3V Module Supply Ground
17	GND	3.3V Module Supply Ground	132	TX6n	CML Input
18	GND	3.3V Module Supply Ground	131	TX6p	CML Input
19	GND	3.3V Module Supply Ground	130	GND	Ground (1)
20	GND	3.3V Module Supply Ground	129	TX5n	CML Input
21	VND_IO_A	Module Vendor I/O, NC	128	TX5p	CML Input
22	VND_IO_B	Module Vendor I/O, NC	127	GND	3.3V Module Supply Ground
23	GND	3.3V Module Supply Ground	126	TX4n	CML Input
24	(TX_MCLKn)	Tx Monitor Clock Output	125	TX4p	CML Input
25	(TX_MCLKp)	Tx Monitor Clock Output	124	GND	3.3V Module Supply Ground
26	GND	3.3V Module Supply Ground	123	TX3n	CML Input
27	VND_IO_C	Module Vendor I/O, must not connect at host board	122	TX3p	CML Input
28	VND_IO_D	Module Vendor I/O, must not connect at host board	121	GND	3.3V Module Supply Ground
29	VND_IO_E	Module Vendor I/O, must not connect at host board	120	TX2n	CML Input
30	PRG_CNTL1	Input LVCOMS	119	TX2p	CML Input

31	PRG_CNTL2	Input LVCOMS	118	GND	3.3V Module Supply Ground
32	PRG_CNTL3	Input LVCOMS	117	TX1n	CML Input
33	PRG_ALRM1	Output LVCOMS	116	TX1p	CML Input
34	PRG_ALRM2	Output LVCOMS	115	GND	3.3V Module Supply Ground
35	PRG_ALRM3	Output LVCOMS	114	TX0n	CML Input
36	TX_DIS	“1” or NC: transmitter disabled “0”: transmitter enabled	113	TX0p	CML Input
37	MOD_LOPWR	“1” or NC: module is low power(safe) mode “0”: power-on enabled	112	GND	3.3V Module Supply Ground
38	MOD_ABS	“1” or NC: module absent “0”: module present	111	GND	3.3V Module Supply Ground
39	MOD_RSTn	“0”: resets the module “1” or NC: module enabled	110	NC	Not Connected
40	RX_LOS	“1”: low optical signal “0”: normal condition	109	NC	Not Connected
41	GLB_ALRMn	Global Alarm “0”: alarm condition in any MDIO Alarm register “1”: no alarm condition	108	GND	3.3V Module Supply Ground
42	PRTADR4	1.2V CMOS Input, MDIO Physical port address bit 4	107	RX9n	CML Output
43	PRTADR3	1.2V CMOS Input, MDIO Physical port address bit 3	106	RX9p	CML Output
44	PRTADR2	1.2V CMOS Input, MDIO Physical port address bit 2	105	GND	3.3V Module Supply Ground
45	PRTADR1	1.2V CMOS Input, MDIO Physical port address bit 1	104	RX8n	CML Output
46	PRTADR0	1.2V CMOS Input, MDIO Physical port address bit 0	103	RX8p	CML Output
47	MDIO	1.2V CMOS I/O, Management Data I/O bi-directional data	102	GND	3.3V Module Supply Ground
48	MDC	1.2V CMOS Input, Management Data Clock	101	RX7n	CML Output
49	GND	3.3V Module Supply Ground	100	RX7p	CML Output
50	VND_IO_F	Module Vendor I/O, Not Connected Internally	99	GND	3.3V Module Supply Ground
51	VND_IO_G	Module Vendor I/O, Not Connected Internally	98	RX6n	CML Output
52	GND	3.3V Module Supply Ground	97	RX6p	CML Output
53	VND_IO_H	Module Vendor I/O, Not Connected Internally	96	GND	3.3V Module Supply Ground
54	VND_IO_J	Module Vendor I/O, Not Connected Internally	95	RX5n	CML Output
55	GND	3.3V Module Supply Ground	94	RX5p	CML Output
56	GND	3.3V Module Supply Ground	93	GND	3.3V Module Supply Ground
57	GND	3.3V Module Supply Ground	92	RX4n	CML Output
58	GND	3.3V Module Supply Ground	91	RX4p	CML Output
59	GND	3.3V Module Supply Ground	90	GND	3.3V Module Supply Ground
60	3.3V	3.3V Module Supply Voltage	89	RX3n	CML Output
61	3.3V	3.3V Module Supply Voltage	88	RX3p	CML Output
62	3.3V	3.3V Module Supply Voltage	87	GND	3.3V Module Supply Ground
63	3.3V	3.3V Module Supply Voltage	86	RX2n	CML Output
64	3.3V	3.3V Module Supply Voltage	85	RX2p	CML Output
65	3.3V	3.3V Module Supply Voltage	84	GND	3.3V Module Supply Ground
66	3.3V	3.3V Module Supply Voltage	83	RX1n	CML Output
67	3.3V	3.3V Module Supply Voltage	82	RX1p	CML Output
68	3.3V	3.3V Module Supply Voltage	81	GND	3.3V Module Supply Ground

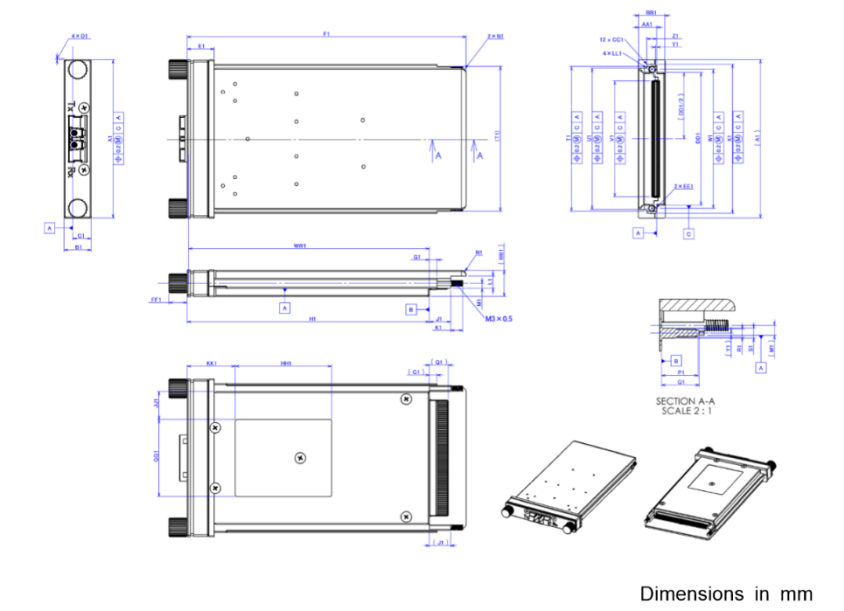
69	3.3V	3.3V Module Supply Voltage	80	RX0n	CML Output
70	GND	3.3V Module Supply Ground	79	RX0p	CML Output
71	GND	3.3V Module Supply Ground	78	GND	3.3V Module Supply Ground
72	GND	3.3V Module Supply Ground	77	(RX_MCLKn)	Rx Monitor Clock Output
73	GND	3.3V Module Supply Ground	76	(RX_MCLKp)	Rx Monitor Clock Output
74	GND	3.3V Module Supply Ground	75	GND	3.3V Module Supply Ground

MECHANICAL DRAWING

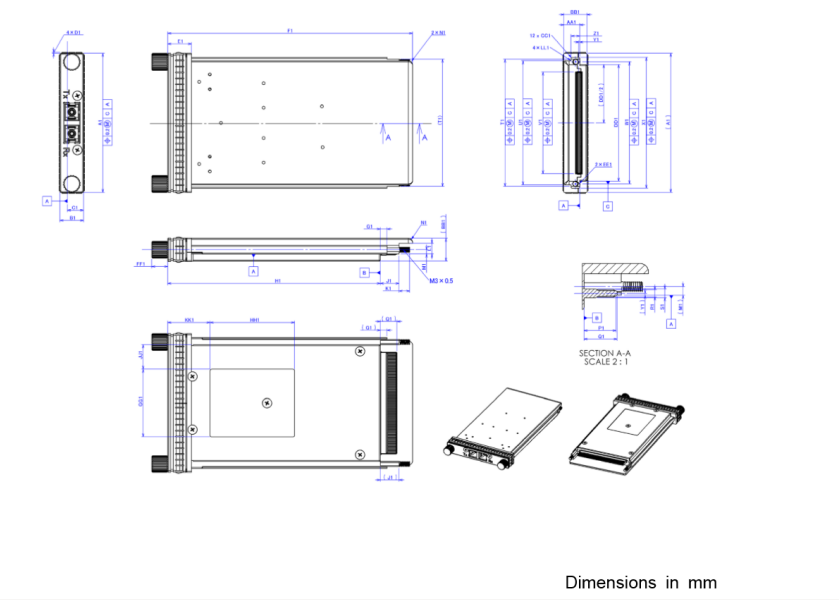
LC ANGLED WITH FLAT TOP PACKAGE DRAWING



LC WITH FLAT TOP PACKAGE DRAWING



SC WITH FLAT TOP PACKAGE DRAWING



Dimensions in mm