SO-QSFP-eSR4

QSFP, 40GBase-SR, 850nm, MM, 300m@OM3, MPO

OVERVIEW

The SO-QSFP-eSR4 is a parallel 40 Gbps Quad Small Form-factor Pluggable (QSFP+) optical module. It provides increased port density and total system cost savings. The QSFP+ full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10 Gbps operation for an aggregate data rate of 40 Gbps on 300 meters of OM3 multi-mode fiber. An optical fiber ribbon cable with an MTP/MPO connector can be plugged into the QSFP+ module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually can't be twisted for proper channel to channel alignment. Electrical connection is achieved through a pluggable 38-pin IPASS® connector. The module operates via a single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference. The module offers very high functionality and feature integration, accessible via a two-wire serial interface.

PRODUCT FEATURES

- 4 independent full-duplex channels
- Up to 11.2 Gbps data rate per wavelength
- MTP/MPO optical connector
- QSFP+ MSA compliant
- Digital diagnostic capabilities
- Up to 300 m transmission on OM3 multimode ribbon fiber
- CML compatible electrical I/O
- Single +3.3V power supply
- Operating case temperature: 0~70oC
- XLPPI electric interface
- Maximum power consumption 1.5W
- RoHS-6 compliant

ORDERING INFORMATION

Part Number	Description
SO-QSFP-eSR4	QSFP, 40GBase-SR, 850nm, MM, 300m@OM3, MPO

APPLICATIONS

- Rack-to-Rack
- Data Center
- Infiniband QDR, DDR and SDR
- 40G Ethernet

FUNCTIONAL DIAGRAM

This product converts parallel electrical input signals into parallel optical signals, by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 10 Gbps per channel. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP+ module must be used.

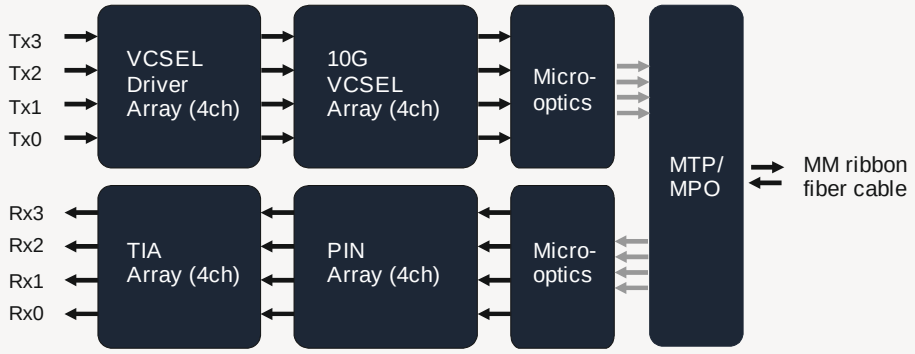


Figure 1. Functional diagram

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground though a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

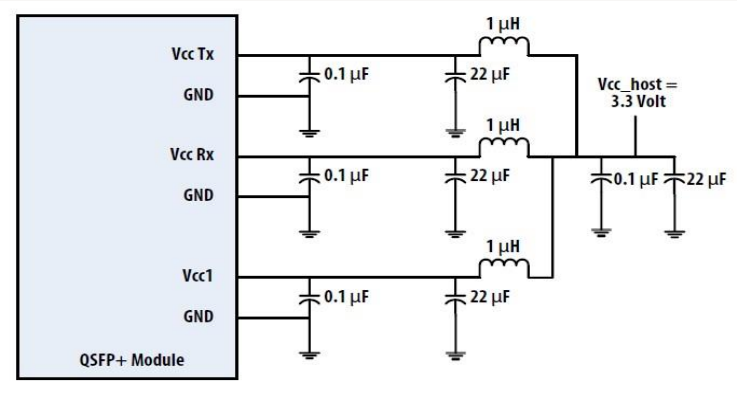
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	*Ts*	-40	+85	degC
Operating Case Temperature	TOP	0	+70	degC
Power Supply Voltage	*VCC*	-0.5	3.6	V
Relative Humidity (non-condensation)	*RH*	0	85	%
Damage Threshold, each Lane	*THd*	3.4		dBm

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	TOP	0		70	degC
Power Supply Voltage	*Vcc*	3.135	3.3	3.465	V
Data Rate, each Lane			10.3125	11.2	Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance (OM3)	D			300	m

RECOMMENDED POWER SUPPLY FILTER



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Power Consumption				1.5	W
Supply Current	*Icc*			450	mA
Transceiver Power-on Initialization Time				2000	ms

ELECTRICAL CHARACTERISTICS – TRANSMITTER (EACH LANE)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single-ended Input Voltage Tolerance (Note 2)		-0.3		4.0	V	Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance (RMS)		15			mV	
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	$V_{in,pp}$	180		1200	mV_{pp}	
Differential Input Impedance	Z_{in}	90	100	110	Ohm	
Differential Input Return Loss		See IEEE 802.3ba 86A.4.1.1			dB	10MHz - 11.1GHz
J2 Jitter Tolerance	J_{t2}	0.17			UI	
J9 Jitter Tolerance	J_{t9}	0.29			UI	
Data Dependent Pulse Width Shrinkage (DDPWS) Tolerance		0.07			UI	
Eye Mask Coordinates {X1, X2,		0.11, 0.31			UI	Hit Ratio = $5x10^{-5}$
Y1, Y2}		95, 350			mV	

ELECTRICAL CHARACTERISTICS – RECEIVER (EACH LANE)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single-ended Output Voltage Threshold		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage (RMS)				7.5	mV	
Differential Output Voltage Swing	$V_{out,pp}$	600		800	mV_{pp}	
Differential Output Impedance	z_{out}	90	100	110	Ohm	
Termination Mismatch at 1MHz				5	%	
Differential Output Return Loss		See IEEE 802.3ba 86A.4.2.1			dB	10MHz - 11.1GHz
Common mode Output Return Loss		See IEEE 802.3ba 86A.4.2.2			dB	10MHz - 11.1GHz
Output Transition Time		28			ps	20% to 80%
J2 Jitter Tolerance	J_{o2}			0.42	UI	
J9 Jitter Tolerance	J_{o9}			0.65	UI	
Eye Mask Coordinates {X1, X2,		0.29, 05			UI	Hit Ratio = $5x10^{-5}$
Y1, Y2}		150, 425			mV	

Notes:

1. Power-on initialization time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

OPTICAL CHARACTERISTICS – TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Centre Wavelength	λ_0	840	850	860	nm	
RMS Spectral Width	$\Delta\lambda rms$		0.5	0.65	nm	
Average Launch Power (each Lane)	P_{AVG}	-7.5		1.0	dBm	
Optical Modulation Amplitude (OMA) (each Lane)	P_{OMA}	-2.8		3.0	dBm	
Difference in Launch Power between any Two Lanes (OMA)	*Ptx,diff*			4.0	dB	
Peak Power (each Lane)	P_{Pt}			4.0	dBm	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane	*OMATDP*	-6.5			dBm	
TDP (each Lane)				3.5	dB	
Extinction Ratio	*ER*	3			dB	
Relative Intensity Noise	*RIN*			-128	dB/Hz	12dB reflection
Optical Return Loss Tolerance	$_{TOL}$			12	dB	
Encircled Flux		>86% at 19um <30% at 4.5um				
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.23, 0.34, 0.43, 0.27, 0.35, 0.4}				
Average Launch Power OFF (each Lane)	P_{off}			-30	dBm	

Note: Transmitter optical characteristics are measured with a single mode fiber.

OPTICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Centre Wavelength	λ_0	840	850	860	nm	
Damage Threshold (each Lane)	$_{Thd}$	3.4			dBm	3
Average Power at Receiver Input (each Lane)		-9.9		+2.4	dBm	
Receiver Reflectance	R_R			-12	dB	
Receive Power (OMA) (each Lane)				3	dBm	
Stressed Receiver Sensitivity (OMA) (each Lane)				-7.5	dBm	4
Receiver Sensitivity (OMA) (each Lane)	*SEN*			-11.1	dBm	
Peak Power (each Lane)	*PPR*			4.0	dBm	
LOS Assert	LOS_A	-30			dBm	
LOS Deassert	LOS_D			-12	dBm	
LOS Hysteresis	LOS_H	0.5			dB	
Vertical Eye Closure Penalty (each Lane)			1.9		dB	
Stressed Eye J2 Jitter (each Lane)			0.3		UI	
Stressed Eye J9 Jitter (each Lane)			0.47		UI	
OMA of each aggressor lane			-0.4		dBm	

Note: Receiver optical characteristics are measured with a multimode fiber.

DIGITAL DIAGNOSTIC FUNCTIONS

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Temperature monitor absolute error	DMI_{TEMP}	-3		3	deg. C	Over operating temp
Supply voltage monitor absolute error	DMI_{VCC}	-0.15		0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_{RX_CH}	-2		2	dB	1
Channel Bias current monitor	DMI_{Ibias_CH}	-10%		10%	mA	Ch1~Ch4
Channel TX power monitor absolute error	DMI_{TX_CH}	-2		2	dB	1

Note 1: Due to measurement accuracy of different multi-mode fibers, there could be an additional ±1dB fluctuation, or ± 3dB total accuracy.

MODE-CONDITIONING PATCH CABLE

Figure 2. shows the orientation of the multi-mode facets of the optical connector.

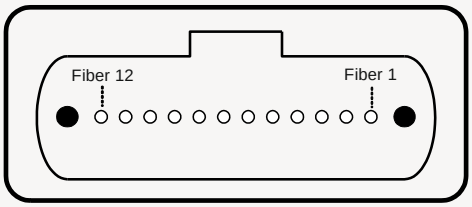


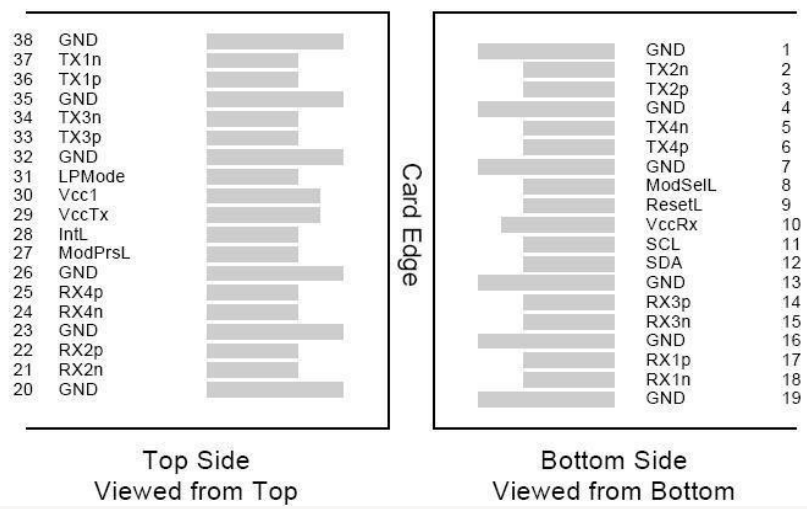
Figure 2. Optical connector

PATCH CABLE PIN DESCRIPTION

Fiber	Description	PIN	Description
1	Rx (0)	7	Not used
2	Rx (1)	8	Not used
3	Rx (2)	9	Tx (3)
4	Rx (3)	10	Tx (2)
5	Not used	11	Tx (1)
6	Not used	12	Tx (0)

PIN ASSIGNMENT AND FUNCTION DEFINITIONS

PIN ASSIGNMENT



PIN DEFINITION

PIN	Signal Name	Description	PIN	Signal Name	Description
1	GND	Ground (1)	20	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input	21	Rx2n	CML-O Receiver 2 Inverted Data Output
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input	22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
4	GND	Ground (1)	23	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input	24	Rx4n	CML-O Receiver 4 Inverted Data Output
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input	25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
7	GND	Ground (1)	26	GND	Ground (1)
8	ModSelL	LVTLL-I Module Select	27	ModPrsL	Module Present
9	ResetL	LVTLL-I Module Reset	28	IntL	Interrupt
10	$V_{CC}R_x$	+3.3V Power Supply Receiver (2)	29	V_{CC}Tx	+3.3V Power Supply Transmitter (2)
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock	30	$V_{CC}1$	+3.3V Power Supply
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data	31	LPMode	LVTLL-I Low Power Mode
13	GND	Ground (1)	32	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output	33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
15	Rx3n	CML-O Receiver 3 Inverted Data Output	34	Tx3n	CML-I Transmitter 3 Inverted Data Input
16	GND	Ground (1)	35	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output	36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input
18	Rx1n	CML-O Receiver 1 Inverted Data Output	37	Tx1n	CML-I Transmitter 1 Inverted Data Input
19	GND	Ground (1)	38	GND	Ground (1)

Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. V_{cc}Rx, Vcc1 and V_{cc}Tx are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.

MECHANICAL DRAWING