

# SO-QSFP-LR4-20

QSFP, 40GBase-LR, CWDM, SM, DDM, 10dB, 20km

## OVERVIEW

The SO-QSFP-LR4-20 is a transceiver module designed for 20km optical communication applications. The design is compliant to 40GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 inputs channels of 10Gbps electrical data to 4 CWDM optical signals, and multiplexes them into a single channel for 40Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 40Gb/s input into 4 CWDM channels signals, and converts them to 4 channel output electrical data. The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G694.2. It contains a duplex LC connector for the optical interface and a 148-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be used. The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

## PRODUCT FEATURES

- Compliant to the IEEE 802.3ba(40GBASE-LR4)
- Compliant to the QSFP+ MSA SFF-8436 specification
- Up to 20km over SMF
- DFBs and PIN monitor photodiodes array for transmitter section
- PIN detectors and TIAs array for receiver section
- Four 10Gbps CWDM channels in the 1310nm band
- I<sup>2</sup>C interface with integrated Digital Diagnostic Monitoring (DDM)
- Utilizes two standard LC optical connector
- Operating case temperature: -10°C~+70°C

## APPLICATIONS

- Extended 40GBASE-LR4 Ethernet links
- Infiniband QDR and DDR interconnects client-side
- 40G Telecom connections

## ORDERING INFORMATION

Part Number	Description
SO-QSFP-LR4-20	QSFP, 40GBase-LR, CWDM, SM, DDM, 10dB, 20km

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## FUNCTIONAL DIAGRAM

This product converts the 4-channel 10 Gbps electrical input data into CWDM optical signals by a driven 4-wavelength Distributed Feedback Laser (DFB) array. The light is combined by the MUX as a 40 Gbps data signal, propagating out of the transmitter module from the SMF. The receiver module accepts the 40 Gbps CWDM optical signals input, and de-multiplexes it into 4 individual 10Gbps channels with different wavelengths. Each wavelength channel is collected by a discrete photo diode and output as electric data after being amplified by a TIA. Figure 1 shows the functional block diagram of this product. A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMODE, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP memory map.

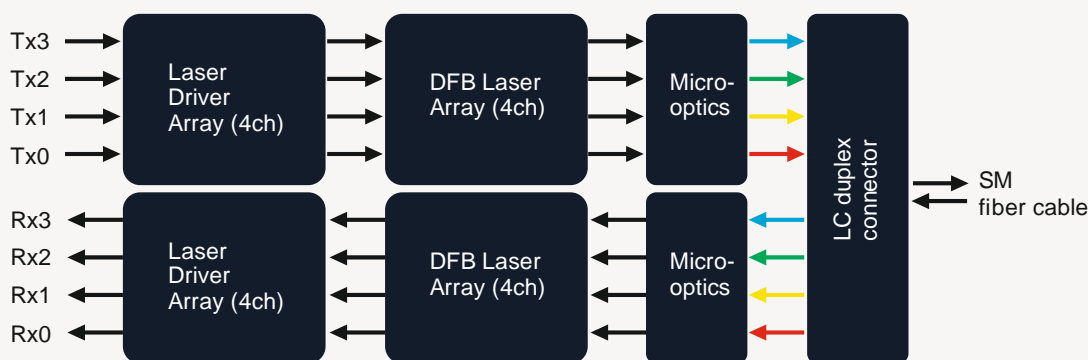


Figure 1. Functional diagram

The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data\_Not\_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset. Low Power Mode (LPMODE) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state. Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	<i>T<sub>s</sub></i>	-40	+75	°C
Supply Voltage	<i>V<sub>cc</sub></i>	-0.5	3.6	V
Operating Relative Humidity	<i>RH</i>	5	85	%

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## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T <sub>c</sub> SO-QSFP-LR4-20	-10		70	°C
Power Supply Voltage	V <sub>cc</sub>	3.15	3.3	3.45	V
Power Supply Current	I <sub>cc</sub>			1000	mA
Power Dissipation	PD			3.5	W
Aggregate Bit Rate	BRAVE		41.25		Gbps
Lane Bit Rate	BRLANE		10.3125		Gbps

## PERFORMANCE SPECIFICATIONS - ELECTRICAL – TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single ended input voltage tolerance		-0.3		4	V	Referred to TP1 signal common
AC common mode input voltage tolerance		15			mV	RMS
Input Impedance (Differential)	Z <sub>in</sub>	85	100	115	ohms	R <sub>in</sub> > 100 kohms @ DC
TX Disable	Disable	V <sub>IH</sub>	2	V <sub>cc</sub> +0.3	V	
	Enable	V <sub>IL</sub>	0	0.8		
TX FAULT	Fault	V <sub>OH</sub>	2.4	V <sub>cc</sub> +0.3	V	
	Normal	V <sub>OL</sub>	0	0.8		

## PERFORMANCE SPECIFICATIONS - ELECTRICAL – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Single ended output voltage		-0.3		4	V	Referred to signal common
AC common mode voltage				7.5	mV	RMS
Termination mismatch at 1MHz				5	%	
Output Impedance (Differential)	Z <sub>out</sub>	85	100	115	ohms	
Output Rise/Fall Time	t <sub>r/f</sub>	30			ps	10%~90%
RX_LOS	LOS	V <sub>oH</sub>	2.4	V <sub>cc</sub> +0.3	V	
	Normal	V <sub>oL</sub>	0	0.8	V	

## OPTICAL AND ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
SMF	L		20		km
Aggregate Bit Rate	BRAVE		41.25		Gbps
Per Lane Bit Rate	BRLANE		10.3125		Gbps

## OPTICAL AND ELECTRICAL CHARACTERISTICS – TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit
Channels wavelength	λ <sub>C</sub>	1264.5	1271	1277.5	nm
		1284.6	1291	1297.5	
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	

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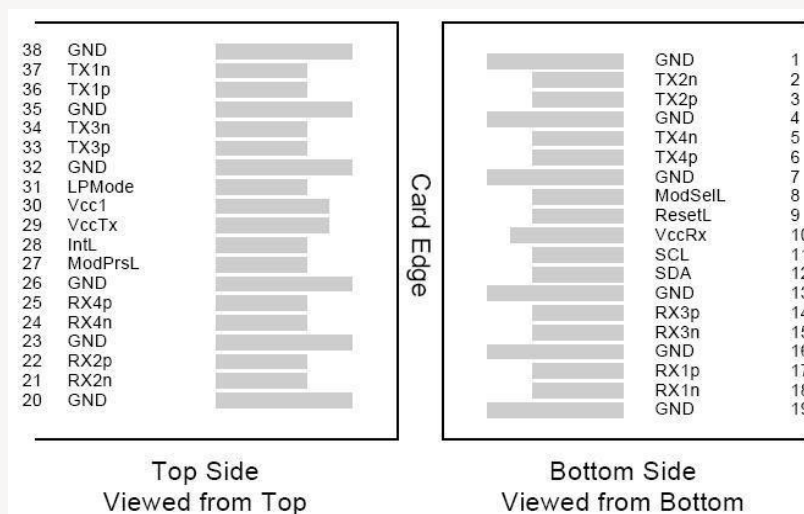
-20dB spectral width	$\Delta\lambda$	1	nm
Average Launch Power, Each Lane	$P_{out/lane}$	-3	2.3 dBm
Per Lane Bit Rate	$E_r$	3.5	dB
Output Optical Eye	IEEE 802.3ba-2010 Compliant		

## OPTICAL AND ELECTRICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit
Channels wavelength	$\lambda_C$	1264.5	1271	1277.5	nm
		1284.6	1291	1297.5	
		1304.5	1311	1317.5	
		1324.5	1331	1337.5	
Damage Threshold		3.3			dBm
Receiver sensitivity in OMA, each lane	$P_{mins}$			-12	dBm
Maximum Receive Power, each lane	$P_{max}$	2.3			dBm
Receiver reflectance	$R_r$			-26	Db
LOS De-Assert	$LOSD$			-11.5	dBm
LOS Assert	$LOSA$	-20			dBm

## PIN ASSIGNMENT AND FUNCTION DEFINITIONS

### PIN ASSIGNMENT



### PIN DEFINITION

PIN	Signal Name	Description	PIN	Signal Name	Description
1	GND	Ground (1)	20	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input	21	Rx2n	CML-O Receiver 2 Inverted Data Output
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input	22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
4	GND	Ground (1)	23	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input	24	Rx4n	CML-O Receiver 4 Inverted Data Output

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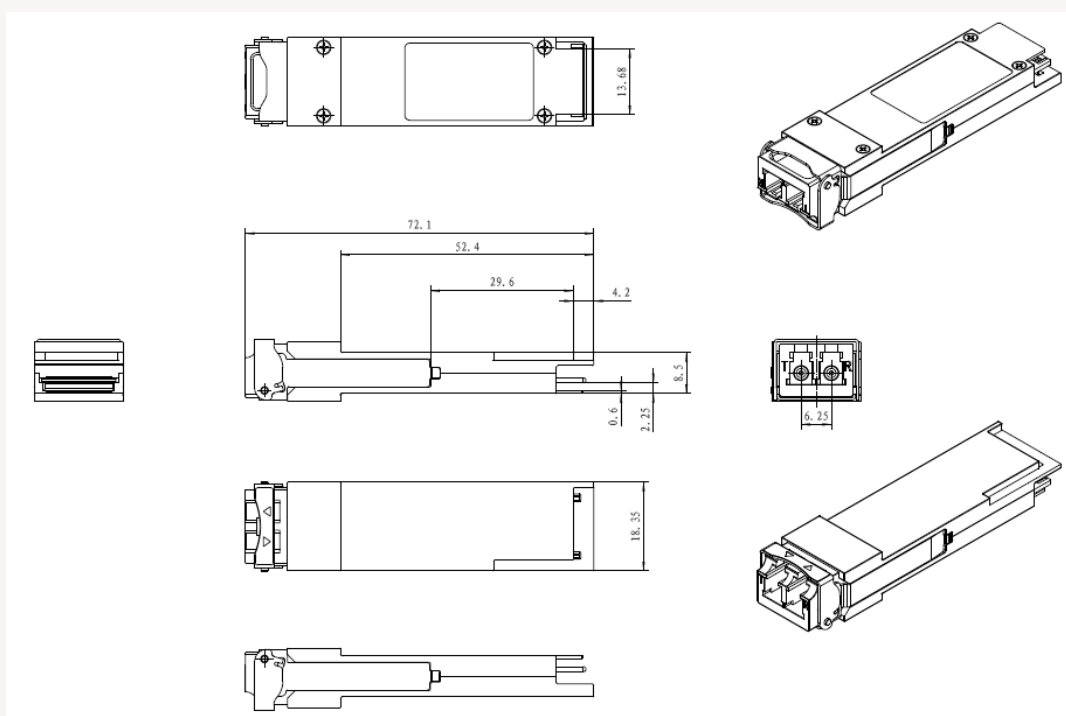
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6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input	25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
7	GND	Ground (1)	26	GND	Ground (1)
8	ModSelL	LVTTLL-I Module Select	27	ModPrsL	Module Present
9	ResetL	LVTTLL-I Module Reset	28	IntL	Interrupt
10	VccRx	+3.3V Power Supply Receiver (2)	29	VccTx	+3.3V Power Supply Transmitter (2)
11	SCL	LVCNOS-I/O 2-Wire Serial Interface Clock	30	Vcc1	+3.3V Power Supply
12	SDA	LVCNOS-I/O 2-Wire Serial Interface Data	31	LPMode	LVTTLL-I Low Power Mode
13	GND	Ground (1)	32	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output	33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
15	Rx3n	CML-O Receiver 3 Inverted Data Output	34	Tx3n	CML-I Transmitter 3 Inverted Data Input
16	GND	Ground (1)	35	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output	36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input
18	Rx1n	CML-O Receiver 1 Inverted Data Output	37	Tx1n	CML-I Transmitter 1 Inverted Data Input
19	GND	Ground (1)	38	GND	Ground (1)

Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.

MECHANICAL DRAWING



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