SO-CFP4-LR4

CFP4, 103/112 Gbps, 1310nm, SM, DDM, 6.3dB, 10km

OVERVIEW

The SO-CFP4-LR4 is a 100Gbps transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE P802.3ba standard. The module converts 4 input channels of 25Gbps electrical data to 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gbps optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gbps optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data. The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high performance cooled LAN WDM EA-DFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant to optical interface with IEEE802.3ba Clause 88 100GBASE-LR4 requirements. The product is designed with form factor, optical/electrical connection and MDIO interface according to the CFP4 Multi-Source Agreement (MSA). The innovative design has all the fibers inside the CFP4 package configured without any splicing or non-permanent connector. Also, fiber routines are neatly organized and fixed inside a stainless steel container

PRODUCT FEATURES

- Hot pluggable CFP4 MSA form factor
- Compliant to IEEE 802.3ba 100GBASE-LR4 and CFP-MSA-CFP4-HW-Specification
- Up to 10km reach for G.652 SMF
- Single +3.3V power supply
- Operating case temperature: 0~70^{o}C
- Transmitter: cooled 4x25 Gbps LAN WDM EML TOSA (1295.56, 1300.05, 1304.58, 1309.14nm)
- Receiver: 4x25Gb/s PIN ROSA
- 4x28G Electrical Serial Interface (CEI-28GVSR)
- MDIO management interface with Digital Diagnostic
- Maximum power consumption 6.0W
- Duplex LC receptacle
- RoHS-6 compliant

ORDERING INFORMATION

Part Number	Description
SO-CFP4-LR4	CFP4, 103/112 Gbps, 1310nm, SM, DDM, 6.3dB, 10km

APPLICATIONS

- 100GBASE-LR4 Ethernet Links
- OTU4

FUNCTIONAL DIAGRAM

This product contains a duplex LC connector for the optical interface and a 56-pin connector for the electrical interface. Figure 1 shows the functional block diagram of this product. The transceiver module receives 4 channels of 25Gbps electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently, each of 4 EML laser driver IC's converts one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled EML lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE802.3ba 100GBASE-LR4 requirements. These 4lane optical signals will be optically multiplexed into a single fiber by a 4-to-1 optical WDM MUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware signal and/or through MDIO module management interface.

The receiver receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by a 1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value is reported through the MDIO section. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

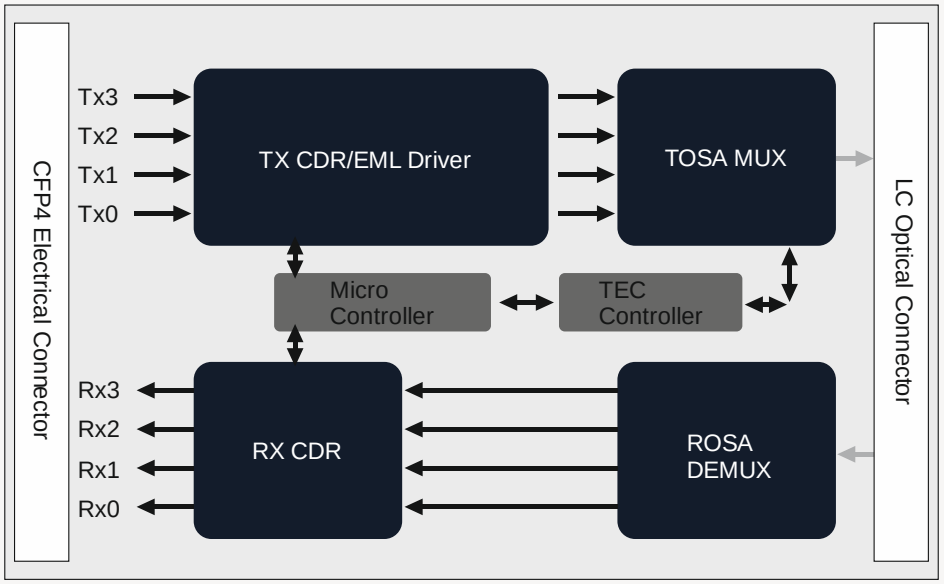


Figure 1. Functional diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Storage Temperature	*Ts*	-40	+85	degC
Operating Case Temperature	T_{OP}	0	70	degC

Power Supply Voltage	Vcc	-0.5	3.6	V
Voltage on LVTTL Input	V_{ilvttl}	-0.5	V_{cc} + 0.3	
LVTTL Output current	I_{olvttl}		15	mA
Voltage on Open Collector Output	V_{oco}	0	6	V
Relative Humidity (non-condensation)	RH	0	85	%
Damage Threshold, each Lane	TH_d	5.5		dBm

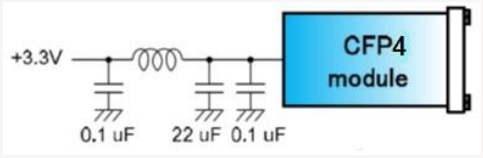
RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	TOP	0		70	degC
Power Supply Voltage	*Vcc*	3.135	3.3	3.465	V
Power Supply Noise	V_{rip}			2	% DC 1MHz
				3	% DC 1- 10MHz
Data Rate, each Lane			25.78125		Gb/s, Note 1
			27.9525		Gb/s, Note 2
Control Input Voltage High)		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance with G.652	D	0.002		10	km

Notes:

1. 100GBase-LR4
2. OTU4 with FEC

RECOMMENDED POWER SUPPLY FILTER



ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Power Consumption		-		6.0	W
Supply Current	*Icc*			1.87	A
Low Power Mode Power Dissipation				1	W

ELECTRICAL CHARACTERISTICS – TRANSMITTER (EACH LANE)

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended Input Voltage Tolerance (Note 1)		-0.3		4.0	V
AC Common Mode Input Voltage Tolerance		15			mV
Differential Input Voltage Swing Threshold		50			mVpp
Differential Input Voltage Swing	*Vin.pp*	190		700	mVpp
Differential Input Impedance	*Zin*	90	100	110	Ω

ELECTRICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit
Single-ended Output Voltage		-0.3		4.0	V
AC Common Mode Output Voltage				7.5	mV
Differential Output Voltage Swing	*Vout.pp*	300		850	mVpp
Differential Output Impedance	*Zout*	90	100	110	Ohm
Termination Mismatch at 1Mhz				5	%

Notes:

1. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

OPTICAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Lane Wavelength	*L0*	1294.53	1295.56	1296.59	nm
	L1	1299.02	1300.05	1301.09	nm
	L2	1303.54	1304.58	1305.63	nm
	L3	1308.09	1309.14	1310.19	nm

OPTICAL CHARACTERISTICS – TRANSMITTER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Side-mode Suppression Ratio	*SMSR*	30			dB	
Total Average Launch Power	P_T			10.5	dBm	
Average Launch Power (each Lane)	P_{AVG}	-4.3		4.5	dBm	
Optical Modulation Amplitude (each Lane)	*POMA*	-1.3		4.5	dBm	1
Difference in Launch Power between any two Lanes (OMA)	$P_{tx,diff}$			5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-2.3			dBm	
TDP, each Lane	TDP			2.2	dB	
Extinction Ratio	*ER*	4			dB	
Relative Intensity Noise	*RIN*			-130	dB/Hz	
Optical Return Loss Tolerance	*TOL*			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				2
Average Launch Power OFF (each Lane)	P_{off}			-30	dBm	

Note: Transmitter optical characteristics are measured with a single mode fiber.

OPTICAL CHARACTERISTICS – RECEIVER

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Damage Threshold (each Lane)	*THd*	5.5			dBm	3
Total Average Receive Power				10.5	dBm	
Average Power at Receiver, each Lane		-10.6		4.5	dBm	
Receive Power (OMA) (each Lane)				4.5	dBm	
Receiver Sensitivity (OMA), each Lane	*SEN*			8.6	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-6.8	dBm	4
Difference in Receive Power between any two Lanes (OMA)	$P_{rx,diff}$			5.5	dB	
LOS Assert	*LOSA*		-18		dBm	
LOS Deassert	*LOSD*		-15		dBm	
LOS Hysteresis	*LOSH*	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	F_c			31	GHz	
Vertical Eye Closure Penalty, each Lane			1.8		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	

Note: The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

MDIO INTERFACE

The CFP4 module supports the MDIO interface specified in IEEE802.3ba Clause 45. It supports alarm, control and monitor functions via hardware pins and via an MDIO bus. Upon module initialization, these functions are available. CFP4 MDIO electrical interface consists of 6 wires including 2 wires of MDC and MDIO, as well as 3 Port Address wires, and the Global Alarm wire. MDC is the MDIO Clock line driven by host and MDIO is the bidirectional data line driven by both host and module depending upon the data directions. The CFP4 uses pins in the electrical connector to instantiate the MDIO interface as listed in Table 1. MDIO Interface Pins.

PIN	Symbol	Description	I/O Typ	Logic	"H"	"L"
13	GLB_ALRMn	Global Alarm	O	3.3V LVCMOS	OK	Alarm
17	MDC	MDIO Clock	I	1.2V LVCMOS		
18	MDIO	Management Data Input Output Bi-Directional Data	I/O	1.2V LVCMOS		
19	PRTADR0	MDIO port address bit 0	I	1.2V LVCMOS	per MDIO document	
20	PRTADR1	MDIO port address bit 1	I	1.2V LVCMOS		
21	PRTADR2	MDIO port address bit 2	I	1.2V LVCMOS		

PIN ASSIGNMENT AND FUNCTION DEFINITIONS

PIN ASSIGNMENT

	CFP4 Bottom
1	3.3V_GND
2	3.3V_GND
3	3.3V
4	3.3V
5	3.3V
6	3.3V
7	3.3V_GND
8	3.3V_GND
9	VND_IO_A
10	VND_IO_B
11	TX_DIS *(PRG_CNTL1)*
12	RX_LOS *(PRG_ALRM1)*
13	GLB_ALRMn
14	MOD_LOPWR
15	MOD_ABS
16	MOD_RSTn
17	MDC
18	MDIO
19	PRTADR0
20	PRTADR1
21	PRTADR2
22	VND_IO_C
23	VND_IO_D
24	VND_IO_E
25	GND
26	*(MCLKn)*
27	*(MCLKp)*
28	GND

	CFP4 Top	CFP4 Top ALT1
56	GND	GND
55	TX3n	TX0n
54	TX3p	TX0p
53	GND	GND
52	TX2n	TX1n
51	TX2p	TX1p
50	GND	GND
49	TX1n	TX2n
48	TX1p	TX2p
47	GND	GND
46	TX0n	TX3n
45	TX0p	TX3p
44	GND	GND
43	*(REFCLKn)*	*(REFCLKn)*
42	*(REFCLKp)*	*(REFCLKp)*
41	GND	GND
40	RX3n	RX3p
39	RX3p	RX3n
38	GND	GND
37	RX2n	RX2p
36	RX2p	RX2n
35	GND	GND
34	RX1n	RX1p
33	RX1p	RX1n
32	GND	GND
31	RX0n	RX0p
30	RX0p	RX0n
29	GND	GND

REFCLK (Optional)

MCLK = TX_MCLK + RX_MCLK (Optional)

PIN DEFINITION

PIN	Signal Name	Description	PIN	Signal Name	Description
1	3.3V_GND	3.3V Module Supply Voltage Return Ground, can be separated or tied together with Signal Ground	29	GND	
2	3.3V_GND		30	Rx0p	
3	3.3V	3.3V Module Supply Voltage	31	Rx0n	
4	3.3V		32	GND	
5	3.3V		33	Rx1p	
6	3.3V		34	Rx1n	
7	3.3V_GND		35	GND	
8	3.3V_GND		36	Rx2p	
9	VND_IO_A	Module Vendor I/O A. Do Not Connect	37	Rx2n	
10	VND_IO_B	Module Vendor I/O B. Do Not Connect	38	GND	
11	TX_DIS	Transmitter Disable for all lanes. "1" or NC: Transmitter disabled; "0": transmitter enabled. (Optionally configurable as Programmable Control1 after Reset)	39	Rx3p	
12	RX_LOS	Receiver Loss of Optical Signal. "1": low optical signal; "0": normal condition (Optionally configurable as Programmable Alarm1 after Reset)	40	Rx3n	
13	GLB_ALRMn	Global Alarm. "0": alarm condition in any MDIO Alarm register; "1": no alarm condition, Open Drain, Pull up Resistor on Host	41	GND	
14	MOD_LOPWR	Module Low Power Mode. "1" or NC: module in low power (safe) mode; "0": power-on enabled	42	(REFCLKn)	
15	MOD_ABS	Module Absent. "1" or NC: module absent; "0": module present, Pull up resistor on Host	43	(REFCLKp)	
16	MOD_RSTn	Module Reset. "0": resets the module; "1" or NC: module enabled, Pull down Resistor in Module	44	GND	
17	MDC	Management Data Clock (electrical specs as per IEEE Std 802.3-2012)	45	Tx0p	
18	MDIO	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3ae-2008 and ba-2010)	46	Tx0n	
19	PRTADR0	MDIO Physical Port address bit 0	47	GND	
20	PRTADR1	MDIO Physical Port address bit 1	48	Tx1p	
21	PRTADR2	MDIO Physical Port address bit 2	49	Tx1n	
22	VND_IO_C	Module Vendor I/O C. Do Not Connect	50	GND	
23	VND_IO_D	Module Vendor I/O C. Do Not Connect	51	Tx2p	
24	VND_IO_E	Module Vendor I/O C. Do Not Connect	52	Tx2n	
25	GND		53	GND	
26	(MCLKn)	For optical waveform testing. Not for normal use	54	Tx3p	
27	(MCLKp)	For optical waveform testing. Not for normal use	55	Tx3n	
28	GND		56	GND	

MECHANICAL DRAWING