SO-QSFP-40G-PCUxM

QSFP, 40GBase-CR4, DAC, AWG28, 0.5m to 5m, passive

OVERVIEW

The SO-QSFP-40G-PCUxM (Quad Small Form-factor Pluggable Plus) Cable Assemblies are suitable for very short distances and offer a highly cost-effective way to establish a 40 Gigabit link between QSFP+ ports of QSFP+ switches within racks and across adjacent racks. QSFP+ cables are used for 40 GbE and Infniband standards, to maximize performance.

PRODUCT FEATURES

- Compliant with 40GBASE-CR4 standard
- QSFP+ MSA compliant
- Compliant with QDR/DDR Infiniband data rates
- AWG24-AWG30
- Up to 11.2Gbps data rate per channel
- Up to 10m transmission
- Operating case temperature: 0~70C
- Maximum 3.5W operation power
- RoHS compliant
- SFF-8436

APPLICATIONS

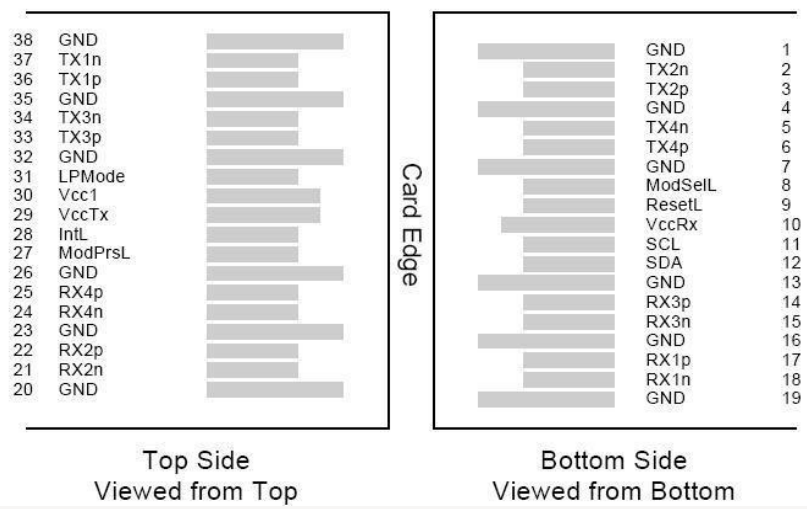
- 40G BASE-CR4 Ethernet links
- Infiniband SDR, QDR and DDR interconnects
- Communications: Switches, Routers, and HBA s
- Networked storage systems
- Computer cluster cross-connect
- Client-side 40G telecom connections

ORDERING INFORMATION

Part Number	Description
SO-QSFP-40G-PCU.5M	QSFP, 40GBase-CR4, DAC, AWG28, 0.5m, passive
SO-QSFP-40G-PCU1M	QSFP, 40GBase-CR4, DAC, AWG28, 1m, passive
SO-QSFP-40G-PCU2M	QSFP, 40GBase-CR4, DAC, AWG28, 2m, passive
SO-QSFP-40G-PCU3M	QSFP, 40GBase-CR4, DAC, AWG28, 3m, passive
SO-QSFP-40G-PCU5M	QSFP, 40GBase-CR4, DAC, AWG24, 5m, passive

PIN ASSIGNMENT AND FUNCTION DEFINITIONS

PIN ASSIGNMENT



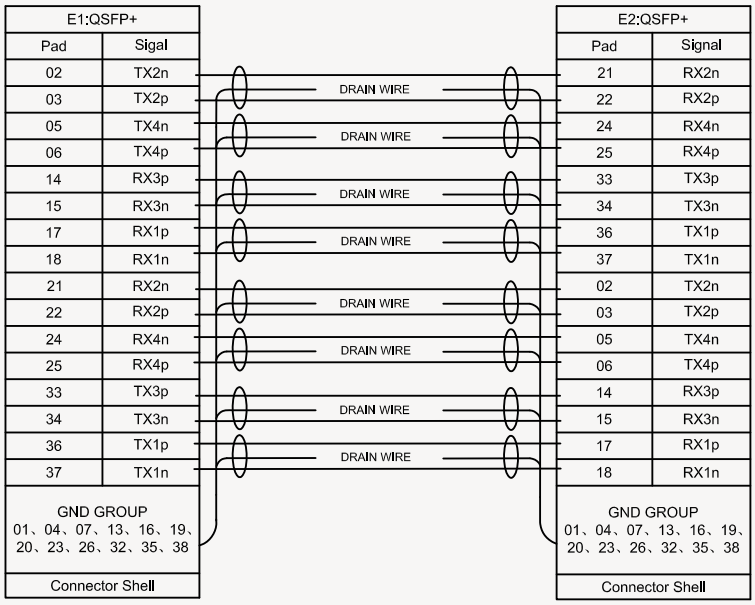
PIN DEFINITION

PIN	Signal Name	Description	PIN	Signal Name	Description
1	GND	Ground (1)	20	GND	Ground (1)
2	Tx2n	CML-I Transmitter 2 Inverted Data Input	21	Rx2n	CML-O Receiver 2 Inverted Data Output
3	Tx2p	CML-I Transmitter 2 Non-Inverted Data Input	22	Rx2p	CML-O Receiver 2 Non-Inverted Data Output
4	GND	Ground (1)	23	GND	Ground (1)
5	Tx4n	CML-I Transmitter 4 Inverted Data Input	24	Rx4n	CML-O Receiver 4 Inverted Data Output
6	Tx4p	CML-I Transmitter 4 Non-Inverted Data Input	25	Rx4p	CML-O Receiver 4 Non-Inverted Data Output
7	GND	Ground (1)	26	GND	Ground (1)
8	ModSelL	LVTLL-I Module Select	27	ModPrsL	Module Present
9	ResetL	LVTLL-I Module Reset	28	IntL	Interrupt
10	$V_{CC}R_x$	+3.3V Power Supply Receiver (2)	29	V_{CC}Tx	+3.3V Power Supply Transmitter (2)
11	SCL	LVCMOS-I/O 2-Wire Serial Interface Clock	30	$V_{CC}1$	+3.3V Power Supply
12	SDA	LVCMOS-I/O 2-Wire Serial Interface Data	31	LPMode	LVTLL-I Low Power Mode
13	GND	Ground (1)	32	GND	Ground (1)
14	Rx3p	CML-O Receiver 3 Non-Inverted Data Output	33	Tx3p	CML-I Transmitter 3 Non-Inverted Data Input
15	Rx3n	CML-O Receiver 3 Inverted Data Output	34	Tx3n	CML-I Transmitter 3 Inverted Data Input
16	GND	Ground (1)	35	GND	Ground (1)
17	Rx1p	CML-O Receiver 1 Non-Inverted Data Output	36	Tx1p	CML-I Transmitter 1 Non-Inverted Data Input
18	Rx1n	CML-O Receiver 1 Inverted Data Output	37	Tx1n	CML-I Transmitter 1 Inverted Data Input
19	GND	Ground (1)	38	GND	Ground (1)

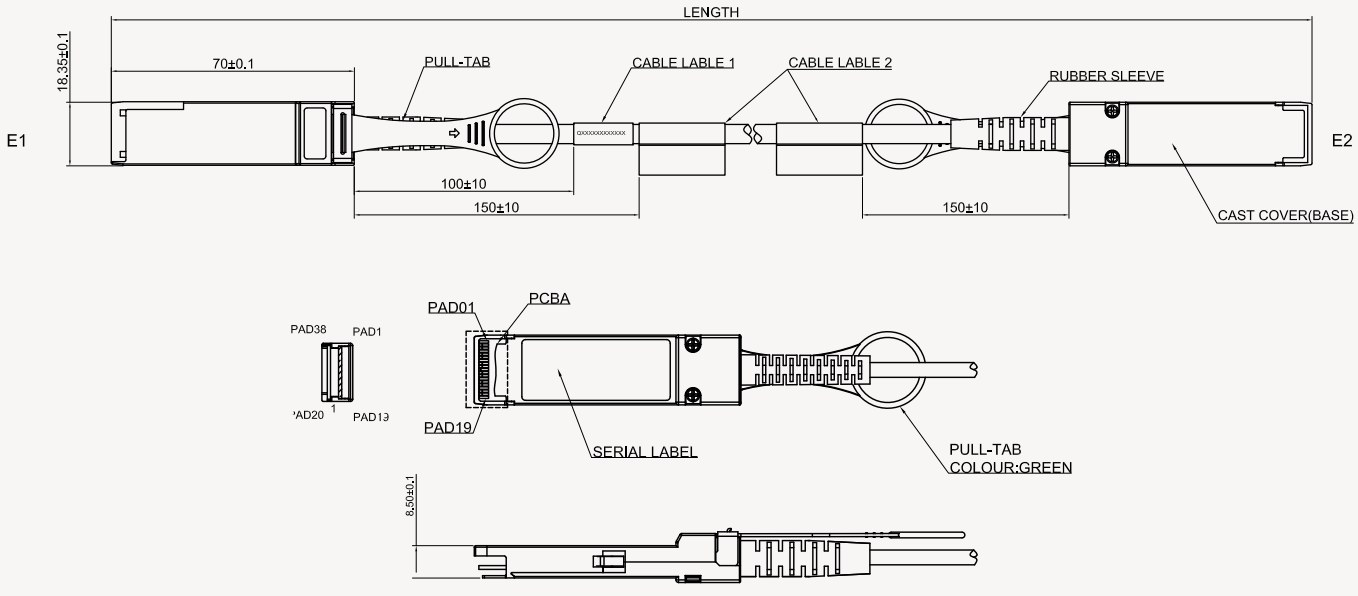
Notes:

1. All Ground (GND) are common within the QSFP+ module and all module voltages are referenced to this potential unless noted otherwise. Connect these directly to the host board signal common ground plane.
2. V_{cc}Rx, Vcc1 and V_{cc}Tx are the receiving and transmission power suppliers and shall be applied concurrently. The connector pins are each rated for a maximum current of 500mA.

CABLE CONNECTION

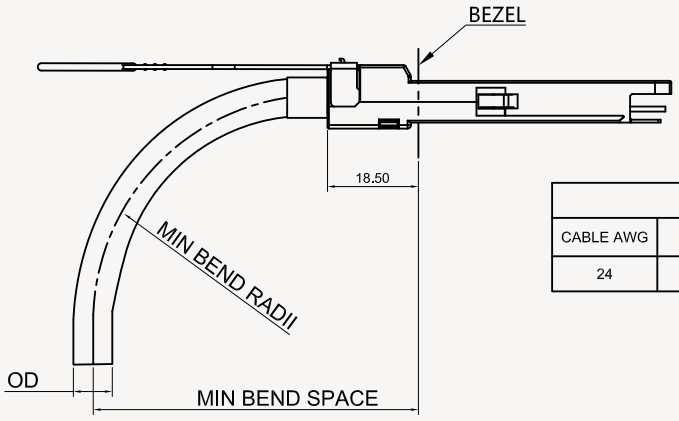


MECHANICAL DRAWING

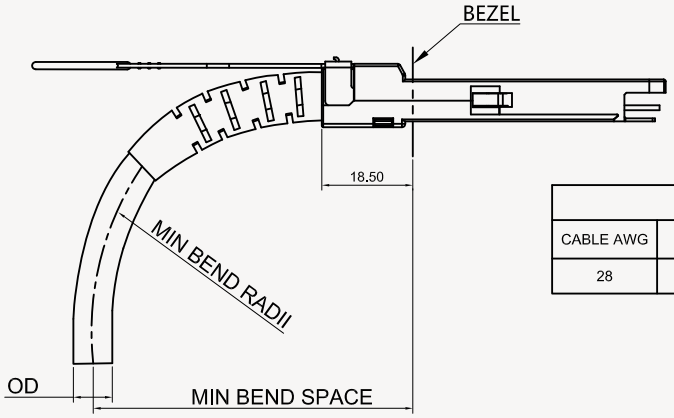


TYPE A

MINIMUM BEND RADIUS



BEND RADII			
CABLE AWG	OD(mm)	MIN BEND RADII(mm)	MIN BEND SPACE
24	9.2	46.0	64.5



BEND RADII			
CABLE AWG	OD(mm)	MIN BEND RADII(mm)	MIN BEND SPACE
28	7.6	38.0	56.5